

FOR IMMEDIATE RELEASE

STATS ChipPAC Introduces Robust Encapsulated Wafer Level Packaging Technology

Innovative package delivers increased durability for mobile devices

Singapore – 28 May 2014 – STATS ChipPAC Ltd. (“STATS ChipPAC” or the “Company” – SGX-ST: STATSchP), a leading provider of advanced semiconductor packaging and test services, today introduced encapsulated Wafer Level Chip Scale Package (eWLCSP™), an innovative packaging technology that raises the industry standard of durability for Wafer Level Chip Scale Packaging (WLCSP).

WLCSP is one of the fastest growing segments in the semiconductor industry driven by mobile electronics that require compact, high performance packages. Although WLCSP is considered a mature technology, there is now an increased sensitivity in the semiconductor industry to reduce the possibility of damage to the package during the surface mount technology (SMT) process. As the industry transitions to more advanced silicon node products, the exposed die that is inherent in the WLCSP design becomes more of a concern due to the fragile dielectric layers.

“WLCSP is a bare die package that is constantly exposed to potential cracking, chipping and handling damages before or during the SMT process. This is particularly true for advanced node products where the die is very thin and dielectric layers are extremely fragile,” said Dr. Han Byung Joon, Executive Vice President and Chief Technology Officer, STATS ChipPAC. “As mobile device manufacturers tighten their technical specifications to reach new levels of reliability in their products, the industry will see more stringent component level and board level reliability (BLR) requirements. eWLCSP™ is a robust packaging solution that cost effectively addresses the increased durability requirements for our customers in advanced silicon nodes down to 28nm.”

eWLCSP™ features a thin protective coating on the four sidewalls of the die, achieving increased durability and reliability within the standard WLCSP size specification. The significant benefit of encapsulation is the light and mechanical protection for the bare die. The protective layer also safeguards the silicon during socket insertion for test. eWLCSP delivers electrical performance that is equivalent to standard WLCSP with proven results in component level reliability (CLR), temperature cycle on board (TCoB) and drop test.

The encapsulation advantages in eWLCSP are the result of STATS ChipPAC’s new FlexLine™ manufacturing method. FlexLine™ is an innovative approach to wafer level manufacturing that seamlessly processes multiple silicon wafer diameters in the same manufacturing line, delivering unprecedented flexibility in producing both fan-out and fan-in packages. Flexline™ is based on STATS ChipPAC’s well established, high volume manufacturing process for fan-out wafer level packaging that provides the ability to scale a device to larger panel sizes for a compelling cost reduction compared to conventional wafer level packaging methods. The FlexLine™ process has been qualified at advanced silicon nodes down to 28nm, ball pitches down to 0.40mm and body sizes as small as 2.5x2.5mm.

Dr. Han continued, “FlexLine is a strong manufacturing platform that enables unique technology enhancements such as eWLCSP and a cost effective manufacturing approach to wafer level packaging. Using the FlexLine method, 200mm incoming wafers can be reconstituted into 300mm or larger panel sizes, providing customers with significant per unit cost reduction as the panel size



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increases. In addition, a conventional WLCSP can be converted to eWLCSP without any silicon design change required, regardless of the current silicon wafer diameter.”

STATS ChipPAC will be presenting on eWLCSP™ and other innovations in wafer level technology, Through Silicon Via (TSV) and advanced flip chip interconnect at the Electronic Components and Technology Conference that is being held May 27th to May 30th, 2014 in Orlando, Florida.

Forward-looking Statements

Certain statements in this release are forward-looking statements that involve a number of risks and uncertainties that could cause actual results to differ materially from those described in this release. Factors that could cause actual results to differ include, but are not limited to, general business and economic conditions and the state of the semiconductor industry; prevailing market conditions; demand for end-use applications products such as communications equipment, consumer and multi-applications and personal computers; decisions by customers to discontinue outsourcing of test and packaging services; level of competition; our reliance on a small group of principal customers; our continued success in technological innovations; pricing pressures, including declines in average selling prices; intellectual property rights disputes and litigation; our ability to control operating expenses; our substantial level of indebtedness and access to credit markets; potential impairment charges; availability of financing; changes in our product mix; our capacity utilisation; delays in acquiring or installing new equipment; limitations imposed by our financing arrangements which may limit our ability to maintain and grow our business; returns from research and development investments; changes in customer order patterns; customer credit risks; disruption of our operations; shortages in supply of key components and disruption in supply chain; inability to consolidate our Malaysia operations into our China operations and uncertainty as to whether such plan will achieve the expected objectives and results; loss of key management or other personnel; defects or malfunctions in our testing equipment or packages; rescheduling or cancelling of customer orders; adverse tax and other financial consequences if the taxing authorities do not agree with our interpretation of the applicable tax laws; classification of our Company as a passive foreign investment company; our ability to develop and protect our intellectual property; changes in environmental laws and regulations; exchange rate fluctuations; regulatory approvals for further investments in our subsidiaries; majority ownership by Temasek Holdings (Private) Limited (“Temasek”) that may result in conflicting interests with Temasek and our affiliates; unsuccessful acquisitions and investments in other companies and businesses; labour union problems in South Korea; uncertainties of conducting business in China and changes in laws, currency policy and political instability in other countries in Asia; natural calamities and disasters, including outbreaks of epidemics and communicable diseases; the continued trading and listing of our ordinary shares on the Singapore Exchange Securities Trading Limited (“SGX-ST”). You should not unduly rely on such statements. We do not intend, and do not assume any obligation, to update any forward-looking statements to reflect subsequent events or circumstances.

About STATS ChipPAC Ltd.

STATS ChipPAC Ltd. (SGX-ST Code: S24) is a leading service provider of semiconductor packaging design, assembly, test and distribution solutions in diverse end market applications including communications, digital consumer and computing. With global headquarters in Singapore, STATS ChipPAC has design, research and development, manufacturing or customer support offices throughout Asia, the United States and Europe. STATS ChipPAC is listed on the SGX-ST. Further information is available at www.statschippac.com. Information contained in this website does not constitute a part of this release.

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